JPL Spec. FM516931

Cassini
Command Data Subsystem

RSDL

Reed-Solomon Downlink
Bus Arbiter
Timing Unit

Functional Specification

Version 3.0
Final

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1. Scope

1.1. Purpose

This document is the primary source of the functional specifications of the space qualified Reed-Solomon Downlink (RSDL) ASIC device for the CASSINI Mission.

This document shall supersede any other RSDL specification documents issued prior to the publication date of this document.

1.2. Description

The RSDL device includes a Reed-Solomon encoder, the Timing unit and the Bus Arbiter. It is fabricated with the HR1060 line of Honeywell RICMOS gate arrays. Due to the gate count limitation, none of the memories associated with the RS encoder are included inside this device.

1.3. Bit Numbering Conventions

Throughout this document, all internal registers assign bit 0 as the MSB to accommodate the MIL-STD-1750A processor, but in the hardware schematics, bit 15 is still the MSB. Refer to [7] for the in-depth description of the bit numbering conventions.

1.4. Abbreviations, Acronyms and Definitions

ASIC	Application Specific Integrated Circuit
C/C	CRAF/Cassini
CDS	Command and Data Subsystem
CMD	SSR Commands
CRC	Critical Controller
DL	Downlink
EFC	Engineering Flight Computer
ISB	Inter-Subassembly Bus
Kbps	10^3 bits per second
LSB	Least Significant Bit
LV	Launch Vehicle
Mbps	10^6 bits per second

MO	Mars Observer
MSB	Most Significant Bit
ns	Nanosecond, 10^{-9} second
PB	SSR Playback
REC	SSR Record
RFS	Radio Frequency Subsystem
RS	Reed-Solomon
RT	Real Time
RTI	Real Time Interrupt
S/C	Spacecraft
SE	Support Equipment
SSR	Solid State Recorder
ST	SSR TLM Status
T0	T0 Umbilical
TCU	Telemetry Control Unit
TLM	Telemetry
TU	Timing chain Unit
RT Transfer Frames	Real time science and engineering data before encoding
SSR Transfer Frames	SSR Playback data before encoding
DL Frames	Frames after encoding. These include the 32-bit synchronization pattern and the original RT, or SSR transfer frames and RS check bits.

2. Applicable Documents

- [1] JPL 699-205-4-2006; May 13, 1993
  C/C Command & Data Subsystem Functional Requirement
- [2] JPL IOM 3484-91-C/C: 2.036
  CDS Constraints: Downlink, Uplink, and Bus Management
- [3] JPL SPEC ES515831
  C/C Engineering Flight Computer Detailed Specification
- [4] JPL SPEC FM515834
  C/C Solid State Recorder Functional Requirement
- [5] Mars Observer Project
- [6] JPL Publication 82-71
  Reed-Solomon Encoders - Conventional vs Berlekamp's Architecture
- [7] JPL IOM 3483-CAS: 4h.003;Rev A
  Bit Numbering Conventions and Domains of Applicability
- [8] CCSDS 100.0-G-1
  Telemetry: Summary of Concept and Rationale

- [9] CCSDS 101.0-B-2
  Telemetry Channel Coding
- [10] CCSDS 102.0-B-2
  Packet Telemetry
- [11] Honeywell SID 12490
  Honeywell Documentation: Design-for-Test Manual
- [12] JPL IOM 3480-CAS:4b.085
  Spacecraft Time Update Process

3. Overview

The RSDL chip includes a hardware RS Encoder which is used to encode transfer frames, the Timing unit which will keep track of the S/C time and the DL frequency and the Bus Arbiter which will arbitrate the access to the ISB bus. A separate memory buffer is used to keep track of the check bits. The encoder design itself is based on a design by E. R. Berlekamp. The code used here is defined as a (255,223) code with the interleaved depth of 5. This code is defined by NASA in the telemetry blue books [8,9,10] with a much more in-depth description given in [6].

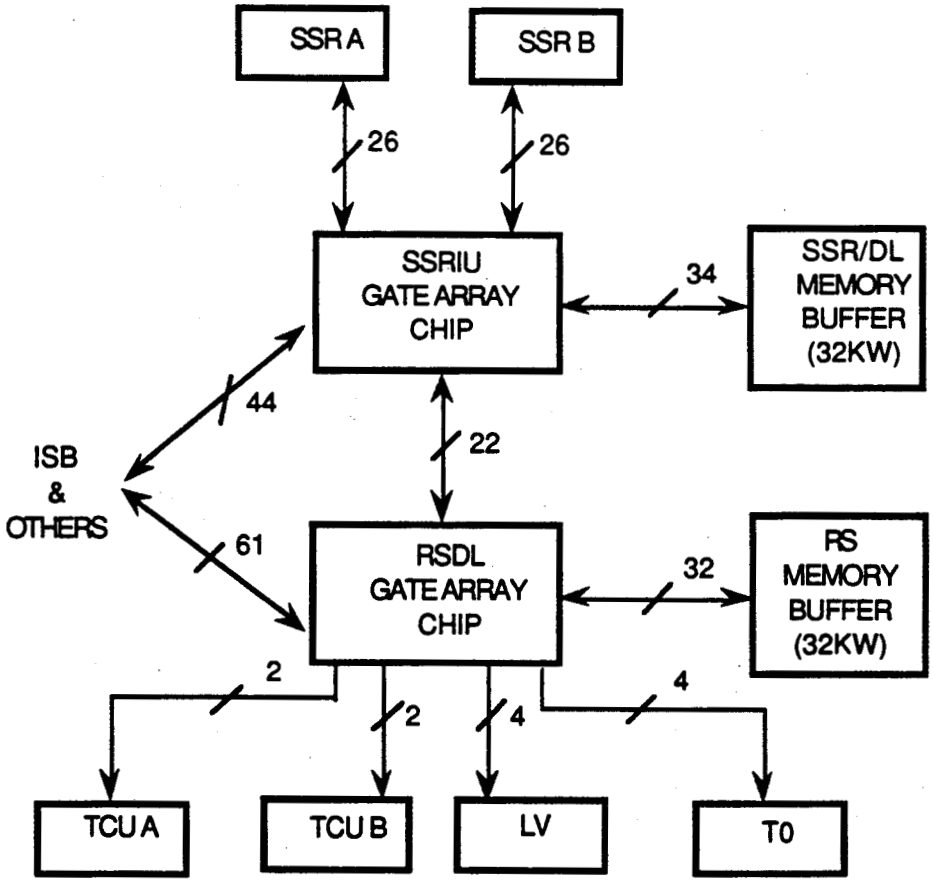


Figure 3.1 External Interface of the SSRIU & RSDL Chips

4. Functional Requirements

The RSDL chips shall provide all the functional capabilities described in the following sections.

4.1. Memory Buffer Interface Requirements

The Read/write cycle of the memory buffer shall be completed within 150ns.

4.2. Downlink Requirements

The design shall meet the following downlink requirements [1].

1. Support the maximum downlink data rate of 249 Kbps.

2. Support the minimum downlink data rate of 5 bps.

3. Generate a DL frame that consists of a 32-bit hardwired synchronization pattern, a RT or SSR transfer frame, and the corresponding RS check bits. The DL data and the clock signal which is six times that of the data rate clock will be sent to both TCUs. It is upto the TCU to select which data and clock signal will be used. The DL data shall be changed at the falling edge of the clock signal.

4. The DL frame and the data rate clock will be sent to T0 along with DEADP and RTI signals. The DL data shall be changed at the rising edge of the data clock.

5. The DL frame and the data rate clock will be sent to LV. ALL signals going to LV I/F shall have a 4 12MHz-cycle pulse width (≈ 334ns) and shall have the waveforms shown in figure 4.2.

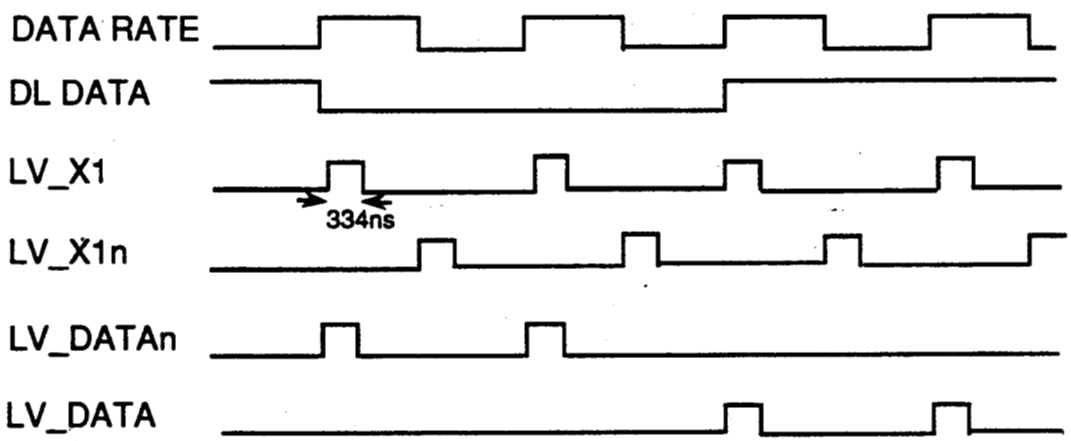


Figure 4.2 Launch Vehicle Interface Timing Waveforms

6. Correlate the S/C time with the first bit of the first frame of every DL buffer.

7. Interleave SSR transfer frames with RT transfer frames.

8. Provide capability to bypass the RS encoding such that a DL frame only consists of the synchronization pattern and the transfer frame which could have a short frame length as well.

4.3. Timing Unit (TU) Requirements

The TU shall meet the following functional requirements [1].

1. The TU shall generate the following critical timing signals:
   8 Hz RTI; Pulse wdith = 1 us,
   8 Hz ARTI; Pulse width = 1 us,
   64Hz signal for EFC; Pulse width = 1 us,
   8 Hz DEADP; Pulse width = 5 ms,
   2048 Hz RELAYP; Pulse width = 1 ms,
   16384 Hz base frequency for S/C clock,
   Programmable 'X12' frequency for RSDL bit timing (max frequency = 5,972,400 Hz)

2. The TU shall store and maintain the S/C time in a 46 bit counter known as the spacecraft (S/C) clock.

3. The LSB of the S/C clock shall have a resolution of 61 microseconds and the entire counter is able to maintain unique time (no rollover) for 136 years.

4. The value of the S/C clock in the prime CDS string may only be changed on ground command. Time is loaded to a resolution of one second.

5. The S/C clock in the backup CDS string shall be resynchronized to the prime CDS string once each second.

6. The TU shall contain a 16 bit 'time stamp' register which stores the LSBs of the S/C clock when the first bit of a new downlink buffer is clocked out of the CDS.

7. The TU shall contain the downlink data rate registers.

4.4. Bus Arbiter (BA) Requirements

The BA shall meet the following functional requirements [1].

1. The BA shall assign the ISB ownership to one of four requesters at a time. The ISB ownership selection shall depend on requester priority, relative bus request timing, and BA operation mode.

2. The BA shall support two mutually exclusive operational modes: the normal mode and the hog mode.

3. In the normal mode, the BA shall employ a simple priority mechanism that grants bus ownership to the highest priority bus master. ISB ownership will not change unless another bus master makes an access request.

   Comment: In Cassini CDS, the highest priority bus master is the EFC.

4. In the hog mode, the BA forces other bus masters off the bus and assigns exclusive use of the bus to the second priority bus master.

   Comment: In Cassini CDS, the second prority bus master is assigned to the XBA DMA controller.

4.5. Inter-Subassembly Bus Requirements

The design shall provide an interface to the ISB which has the maximum bandwidth of 16Mbps. The interface shall only be in slave ISB mode.

4.6. Miscellaneous Requirements

In addition, the design shall provide the following functions.

1. Provide the status of the ASIC chip. All of the internal registers shall be readable by the processor over the ISB.

2. Provide an interface to the cross-strapped TCU. No single point failure within a single CDS string shall prevent communications between an unfailed CDS string and either TCU.

3. All bits which generate interrupts shall also result in status flags being set which allow software to determine the interrupt cause.

5. Design Approach

5.1. Cross-Strapping technique

The cross-strapping scheme as shown in figure 5.1 is used to establish the communication between two CDS strings and the two TCUs. Within a CDS string, both TCU ports are active. Therefore, the TCU needs to select which port is the prime one.

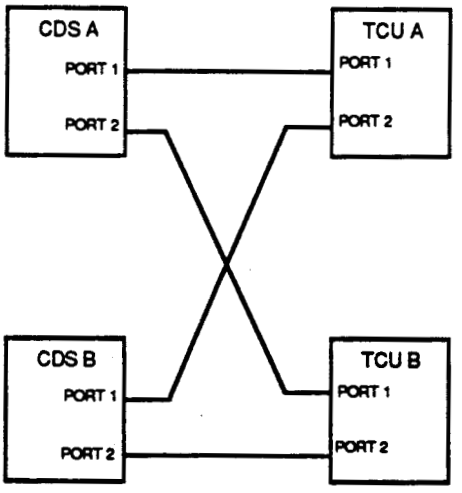


Figure 5.1 CDS & TCU Interconnect

5.2. Memory Map Approach

All internal registers accessed from the ISB is memory mapped. ISB Addresses 1EF500-1EF5FF are reserved for RSDL internal registers. The RS buffer memory which holds the check bits is not memory mapped. This memory can only be accessed by the RS encoder. To increase the fault-tolerance of the memory, the RS buffer memory is divided into 64 segments where any one of them can be selected by the software to store the check bits.

5.3. Adaptation of a Previous Working Design

The RS encoder design is inherited from the Mars Observer project.

5.4. Generic Approach

It is intended to make these devices as generic as possible so they can be reconfigured easily for other flight projects. This is facilitated by the following requirements:

- Keep the transfer frame length, and the number of transfer frames stored in the SSR/DL memory buffer, programmable.

- Let the software decide when to synchronize the DL frame with the RTI.

5.5. Testable Design

The Honeywell Design For Test techniques have been used throughout the design to make it more testable. The in-depth description of these techniques can be found in [11].

6. RSDL Design Description

6.1. RSDL Pin Definition

All signals ending with a "n" are active low. All i/o pads used here are compatible with CMOS devices.

It should also be noticed that the signal **SWRST0n is identical to the SWRST_3n signal in ICD document.**

Pinname	Type	Description
A(7:0)	IN	ISB Address Bus (256W).
DP	IO	ISB Data Parity.
D(15:0)	IO	ISB Data Bus.
DPEn	OUT	ISB Data Parity Error. It indicates that illegal ISB data parity has been detected during the current ISB write cycle.
AREn	OUT	ISB Address Range Error. It indicates that ISB is accessing an undefined register.
ADVn	IN	ISB Address Valid.
RDIR	IN	ISB Read Direction. It indicates an ISB read cycle when it is high, an ISB write cycle when it is low.
DTACKn	OUT	ISB Data Transfer Acknowledge. It indicates the data transfer is complete.
RSDL_INTn	OUT	RSDL Interrupt line. It is asserted when an internal error has been detected. The cause of the interrupt can be seen in the Interrupt Register.
M11.9_CLK	IN	11.9448MHZ clock comes from the crystal.
RDECODE	IN	Select Local Register. ISB accesses RSDL internal register. This decoded line comes from the HCD/CRC device.
PORn	IN	Power On Reset. This signal comes from HCD/CRC.
SWRST0n	IN	Software Reset 0. This signal comes from HCD/CRC.
RSA(12:0)	OUT	RS Memory Buffer Address Bus.
RSD(15:0)	IO	RS Memory Buffer Data Bus.
RSCSn	OUT	RS Memory Buffer Chip Select.
RSWEn	OUT	RS Memory Buffer Write Enable.
RSOEn	OUT	RS Memory Buffer Output Enable.

DLA_DATA	OUT	Downlink Data to TCU A.
DLA_X6	OUT	Six times the Downlink Data Rate Clock to TCU A.
DLB_DATA	OUT	Downlink Data to TCU B.
DLB_X6	OUT	Six times the Downlink Data Rate Clock to TCU B.
T0_DATA	OUT	Downlink Data to T0 (open collector).
T0_DATAn	OUT	Downlink Data in reverse polarity to T0 (open collector).
T0_X1	OUT	One times the Downlink Data Rate Clock to T0 (open collector).
T0_X1n	OUT	One times the Downlink Data Rate Clock in reverse polarity to T0 (open collector).
LV_DATA	OUT	Downlink Data to LV interface.
LV_DATAn	OUT	Downlink Data in reverse polarity to LV interface.
LV_X1	OUT	One times the Downlink Data Rate Clock to LV interface.
LV_X1n	OUT	One times the Downlink Data Rate Clock in reverse polarity to LV interface.
BUFSEL	OUT	Buffer Select for the DL buffer. 0 selects the A buffer, 1 selects the B buffer. This signal goes to the SSRIU device.
BUFSWAP	OUT	Swap the DL buffer. This signal goes to the SSRIU device.
EOB	IN	End of the DL buffer. This signal comes from the SSRIU device. It indicates that the end of the DL buffer has been reached.
RSTn	OUT	Synchronous Reset. This is the combined Hardware/Software reset. This signal goes to the SSRIU device.
DLREQn	OUT	DL request for memory read. This signal goes to the SSRIU device.
DLDONEn	IN	DL request has been served. This signal comes from the SSRIU device.
DLDATA(15:0)	IN	DL Data bus. This bus comes from the SSRIU device.
PRIME	IN	Prime indicates whether this CDS string is a primary string or not. This signal comes from the HCD/CRC chip.
RSHEALTH	IN	Redundant String Health. This signal comes from HCD/CRC chip
GNDUE	IN	Ground Update Enabled. It is used to indicate if the ground wants to update the S/C time. It is a CRC bit.
XRTIn	IN	Cross-strapped RTI. This signal comes from the XBA chip.
RTIn	OUT	Real Time Interrupt. The pulse width is 1.004μs at a frequency of 8 Hz.
ARTIn	OUT	ARTIn occurs 5ms before RTI. The pulse width is 1.004μs.
EFCn	OUT	64.005 Hz clock with 1.004μs pulse width.
DEADP	OUT	Dead Period. It is the time between the end of the ARTI and the beginning of the RTI.
RELAYP	OUT	2048.148 Hz clock with 1.004μs pulse width.
SE_DP	OUT	DEADP sent to SE (open collector).

SE_DPn	OUT	DEADPn to SE (open collector).
SE_RTI	OUT	RTI to SE (open collector).
SE_RTIn	OUT	RTIn to SE (open collector).
BRn(3:0)	IN	ISB Bus Request. These signals come from the XBA and the EFC.
BGn(3:0)	OUT	ISB Bus Grant. These signals will go to the XBA and the EFC.
BGABTn	OUT	Bus Grant Abort.
HOG	IN	The HOG signal forces the Bus Arbiter to only grant the ISB bus to the XBA.
EX_MSEL	IN	External Memory Select. This is the MDECODE of the SSRIU chip. It indicates the SSR/DL memory of the SSRIU being accessed.
EX_RSEL	IN	External Register Select. This is the RDECODE of the SSRIU chip. It indicates an internal register of the SSRIU being accessed.
EN_DTACKn	OUT	Enable DTACKn. This signal will not be used on board.
ISB1DDIR	OUT	ISB Data Bus Direction for 2A1 Board. This signal controls 2A1 ISB Data bus directions. It is a delay version of RDIR.
XBA_ADENn	OUT	XBA Address Enable. This signal will enable 2A2 board Address bus when XBA is the bus master.
XBA_ADDIR	OUT	XBA Address bus Direction. This signal will control the 2A2 board Address bus direction. A "1" signifies that the EFC is the ISB master. A "0" signifies that the XBA/BC is the ISB master.

Total: 130 pins + 6 Honeywell Design For Test pins.

6.2. RSDL Internal Registers Description

Register 0 is addressed by the least significant address of the memory range reserved for the RSDL registers. Only 14 registers are used out of 256 reserved for the RSDL. When the software writes to the unused registers, the AREn signal is asserted but no DTACKn is returned to the ISB.

Writing to these registers requires special attention. Most of the registers have a portion of read-only bits, read-write bits and unused bits. Also, a special bitwrite scheme is used for status, control, mask and interrupt registers. In this scheme, the most significant bit has the value to be written to the register. A '1' at all other bits indicates that that bit will be written by the value stored at the MSB, and a '0' indicates that that bit will remain the same.

MSB LSB

-----Write to Register i:	1000	0000	1111	1111
Register i before write:	0000	1111	0000	1111
Register i after write:	0000	1111	1111	1111
-----Write to Register i:	0000	0000	1111	1111
Register i before write:	0000	1111	1111	1111
Register i after write:	0000	1111	0000	0000

All the bits in these registers are classified as followed:

R: *Ordinary read.*
SW: Special write scheme.
W: Ordinary write.
U: Unused bits. Read back 0 and write don't care.

Register 0: ST&CTL(RSDL Status and Control Register)
(1EF500) All bits are equal to 0 except the mask bits after reset. All mask bits are set to 1.

Bit #	Type	Description
0 (MSB)	W	Special bit. This value will be written to all affected bits. Reading of this bit will always get 0 value.
1	SW / R	Buffer Swap Enable. Software sets this bit to enable the swapping of the DL buffer. The hardware will clear this bit when the DL buffer swaps.
2	SW / R	Sync RTI flag. 1 means that the transfer frame needs to be resynchronized when the RTI comes. In normal operation the software sets the flag, and the hardware resets the flag when the RTI occurs.
3	SW / R	Force Buffer bit. When this flag is set and the Sync RTI occurs, the force buffer (see bit 14) will become the DL buffer.
4	SW / R	TU SWTLEN bit. This bit is used in the TU block to load 32 bits into the 32 MSBs of the S/C time. This bit is cleared by hardware after the value has been loaded to the S/C time.
5	SW / R	DL Rate Select bit. This bit is used in the TU block. It selects which predefined value will be used in the Downlink Frequency Generator.
6	SW / R	DL Rate Load bit. This bit is used in the TU block. When it is set and the RTI occurs, the new value will be loaded into the Downlink frequency Generator. This bit is cleared by the hardware after the value has been loaded.
7	SW / R	Disabled Buffer Swap Mask bit. When this bit is set, the Disabled Buffer Swap Interrupt will be masked.
8	SW / R	DPEn Interrupt Mask bit. When it is masked, the DPEn error will be saved in the RSDL Interrupt Register and will assert the DPEn line, but not the RSDL_INTn line. 1 means mask out the corresponding interrupt.

9	SW / R	AREn Interrupt Mask bit. When it is masked, the error will be saved in the RSDL Interrupt Register, and SSRIU will assert the AREn line but not the RSL_INTn line.
10	SW / R	End-of-Buffer Interrupt Mask bit. When it is masked, the interrupt will be saved in the RSDL Interrupt Register, and the RSDL_INTn line will not be asserted.
11	SW / R	Start-of-Buffer Interrupt Mask bit. When it is masked, the interrupt will be saved in the RSDL Interrupt Register, and the RSDL_INTn line will not be asserted.
12	R	Current DL Buffer ID. 0 selects the A Buffer, 1 selects B.
13	R	Current RS Encoding Status. 0 means that the RS encoding is on, otherwise RS encoding is off.
14	SW / R	DL Force Buffer ID. 0 selects the A Buffer. When the Buffer flag is set and Sync RTI occurs, this buffer will become the DL buffer.
15	SW / R	Next RS Encoding Status. When Sync RTI occurs, this encoding status will be used.

Register 1: INTR (RSDL Interrupt Register)

(1EF501) The bits in this registers are set by hardware and cleared by software. The setting of any bits in this register will cause the RSDL interrupt signal (RSDL_INTn) to be raised if the corresponding masking bit (i.e., Bit 7 of Register 0) is not set. After the POR or the software reset, Bit 7 and Bit 11 will be set and all other bits will be cleared. For testing purpose, software is allowed to set the bits in this register in order to invoke interrupt handler routines directly. However, this capability should not be used in normal operation.

Bit #	Type	Description
0 (MSB)	W	Special bit. This value will be written to all affected bits. Here, only 0 value does affect the register. Reading of this bit will always get 0 value.
1:6	U	Spare bits.
7	SW / R	Disabled Buffer Swap Interrupt. It is set when the DL buffer swaps on itself because the Buffer Swap Enable bit (Bit 1 of Reg 0) is disabled.
8	SW / R	DPEn interrupt bit. It is set when the software writes to the RSDL with a data parity error.
9	SW / R	Local AREn interrupt bit. It is set when the software accesses an undefined address.
10	SW / R	Buffer Overflow Interrupt bit. It is set when the DL reads past the end of DL buffer. In that case, the last word of the DL buffer will always be returned.
11	SW / R	Start-of-Buffer interrupt bit. It is set when the DL buffer swaps to another buffer or on itself.
12:15	U	Spare bits.

Register 2: FRINF (Current Frame Information Register)
(1EF502)

Bit #	Type	Description
0 (MSB)	U	Spare bit.
1:3	R	Current DL Buffer Size. It is equal to 0 (8 frames) after reset.
4:5	U	Spare bits.
6:15	R	Current Frame Length in 16-bit words. It is equal to 550 after reset.

Register 3: NXFRINF (Next Frame Information Register)
(1EF503)

Bit #	Type	Description
0 (MSB)	U	Spare bit.
1:3	W/R	Next DL Buffer Size. It will be used when the swap buffer occurs. It is equal to 0 (8 frames) after reset.
4:5	U	Spare bits.
6:15	W/R	Next Frame Length in 16-bit words. It will be used when the swap buffer occurs. It is equal to 550 after reset.

Register 4: RSSEG (RS Segment Register)
(1EF504) All bits are equal to 0 after reset.

Bit #	Type	Description
0:1 (MSB)	U	Spare bits.
2:7	R	Current Segment Number. This is the segment of memory used for RS encoding.
8:9	U	Spare bits.
10:15	W/R	Next Segment Number. It will be used when the swap buffer occurs.

Register 5: SCTL1 (SC Time Load 1 Register)
(1EF505) All bits are reset after PORn, but remain unchanged after software reset. This register is loaded to the SCTR2 (Register 8) at RTI boundaries.

Bit #	Type	Description
0:15	W/R	SC Time Load 1. Load 16 MSB of the SC time.

Register 6: SCTL0 (SC Time Load 0 Register)
(1EF506) All bits are reset after PORn, but remain unchanged after software reset. This register is loaded to the SCTR1 (Register 9) at RTI boundaries.

Bit #	Type	Description
0:15	W/R	SC Time Load 0. Load 16 middle bits of the SC time.

Register 7: SCTR2 (SC Time Read 2 Register)
(1EF507) This register can be loaded by software but not reset by PORn or software reset.

Bit #	Type	Description
0:15	R	SC Time Read 2. Read 16 MSB of the SC time.

Register 8: SCTR1 (SC Time Read 1 Register)
(1EF508) This register can be loaded by software but not reset by PORn or software reset.

Bit #	Type	Description
0:15	R	SC Time Read 1. Read 16 middle bits of the SC time.

Register 9: SCTR0 (SC Time Read 0 Register)
(1EF509) This register can be loaded by software but not reset by PORn or software reset.

Bit #	Type	Description
0:15	R	SC Time Read 0. Read 16 LSB of the SC time.

Register 10: FSTR (FS Time Read Register)
(1EF50A)

Bit #	Type	Description
0:15	R	FS Time Read. Read 16 LSB bits of the SC time at the start of 1ST frame in buffer

Register 11: DLDR1 (DL Data Rate 1 Register)
(1EF50B) All bits are reset after PORn, but remain unchanged after software reset. The downlink data rate in this register will take effect only at RTI boundaries.

Bit # Type Description

0:15	W/R	DL Data Rate Load 1. The two most significant bits of the Downlink Data Rate in 2's complement.

Register 12: (1EF50C) DLDR0 (DL Data Rate 0 Register)
All bits are reset after PORn, but remain unchanged after software reset.

Bit #	Type	Description
0:15	W/R	Dl Data Rate Load 0. 16 LSB bits of the Downlink Data Rate in 2's complement.

Register 13: (1EF50D) Zero Register
(to avoid having LAREn when addressing double words)

Bit #	Type	Description
0:15	R	ALL 0s.

6.3. RSDL Detailed Design Description

Figure 6.3 shows a functional block diagram of the RSDL Chip. Each of these blocks will be described thoroughly in the following subsections.

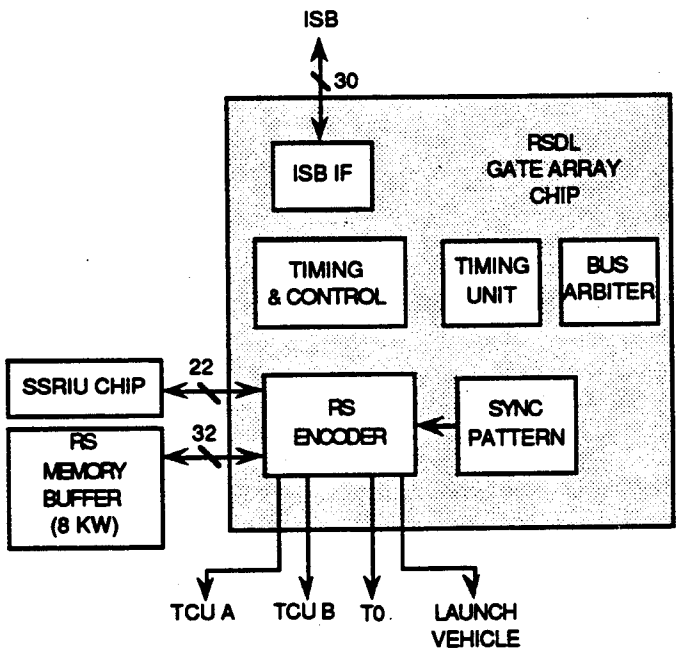


Figure 6.3 Funtional Block Diagram of the RSDL Chip

6.3.1. ISB Interface Block

The RSDL is always in "slave" mode. The interface will include the signals and protocol defined in the EFC specification [3]. The interface block provides the following capabilities:

1) **DTACKn Generation:** The DTACKn signal indicates during a read cycle that the data are stable on pins of the RSDL ASIC. On a write cycle, it indicates that data written by the RSDL ASIC have been captured correctly. The DTACKn is not asserted in the event of the Local Address Range Errors.

2) **Local Address Range Error Generation:** Only 14 registers are used out of the 256 reserved for the RSDL ASIC. When the ISB references the undefined addresses, a Local Address Range Error interrupt is generated which will set the bit #9 of the RSDL Interrupt Register (Register #1), and the RSDL_INTn is asserted. In this event, AREn is asserted but no DTACKn is returned (wait for BTMOn).

3) **DP Generation:** Odd data parity is to be asserted on the ISB during the read cycle.

4) **DP Data Parity Checking:** Odd data parity is checked on write cycle. A write operation is inhibited if a parity error occurs. In the event of a Data Parity Error, both DTACKn and DPEn are asserted. Also when a data parity error occurs, the RSDL_INTn is asserted and the bit #8 of the Interrupt Register is set.

The ISB state flow is shown below:

```
State IDLE:
      if !ADVn & RDECODE then T1
      else IDLE;
State T1:
      if RDIR & !ADVn & RDECODE & AREn then T2R
      else if !RDIR & !ADVn & RDECODE & AREn & DPEn then T2W
      else if !ADVn & RDECODE & !AREn then ERROR
      else if !ADVn & RDECODE & !DPEn & !RDIR then DPERROR
      else IDLE;
State T2W:
      if ADVn # !RDECODE then IDLE
      else T3W;
```

```
State T2R:
      if ADVn # !RDECODE then IDLE
      else T3R;
State T3W:
      if ADVn # !RDECODE then IDLE
      else DTACKW;
State T3R:
      if ADVn # !RDECODE then IDLE
      else DTACKR;
State DTACKW:
      if ADVn then IDLE
      else DTACKW;
State DTACKR:
      if ADVn then IDLE
      else DTACKR;
State ERROR:
      if ADVn then IDLE
      else ERROR;
State DPERROR:
      if ADVn then IDLE
      else DTERROR;
State DTERROR:
      if ADVn then IDLE
      else DTERROR;
```


All unused states are mapped to the IDLE state. The DTACKn is asserted when it is in DTACKW, DTACKR and DTERROR states. Refer to Appendix A for ISB Timing Diagrams.

6.3.2. TU Block

The Timing Unit (TU) block generates clock frequencies used throughout the CDS. It is divided up into three sections, the fixed Timing Chain (TC) section, the Spacecraft Time (SCTime) section, and the Downlink Frequency Generator (DLGen) section. Figure 6.3.2 shows the functionalities of these sections.

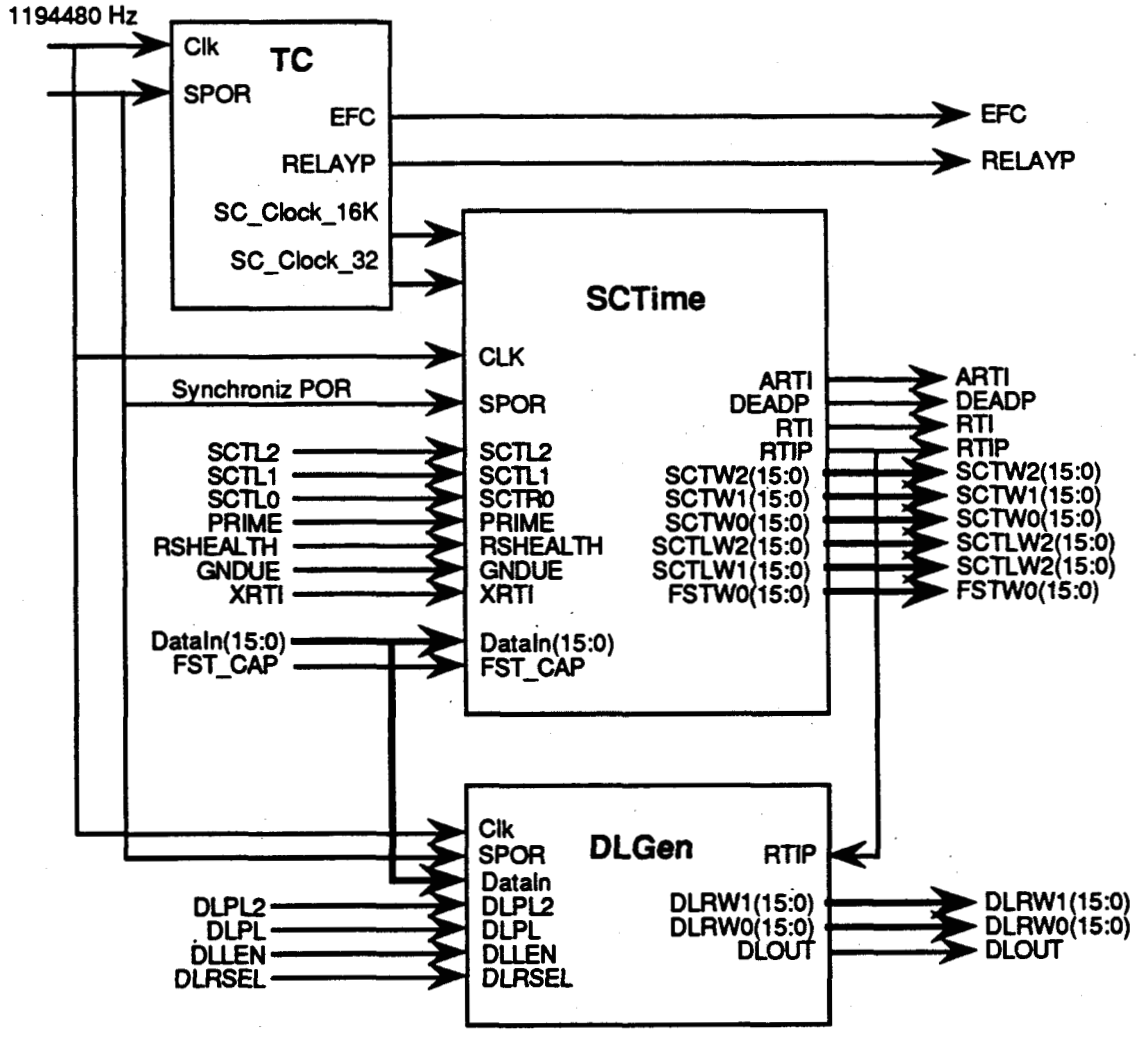


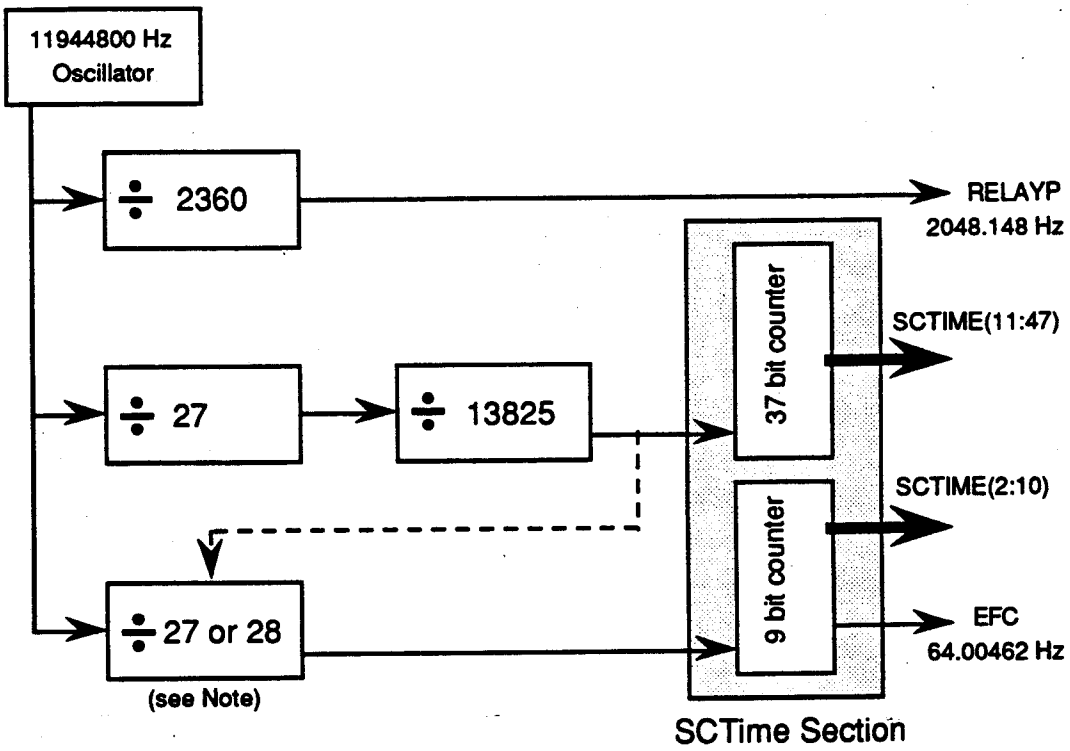
Figure 6.3.2: Three Sections of TU

6.3.2.1 Timing Chain Section

The TC section converts the system clock of 11944800 Hertz into most of the frequencies needed for the CDS. All frequencies generated in this section are derived from a fixed timing chain. The

timing chain block diagram is shown in Figure 6.3.2.1. The frequencies generated are:

- The EFC pulse of 64.005 Hz with a 1.004 μs pulse width.
- A 32 Hz signal used internally by the spacecraft time section.
- A 16385.185 Hz signal used internally by the spacecraft time section.
- A 2048.148 Hz, 1.004 μs pulse width RELAYP signal used by the HCD CRC relays.



Note: This counter divides 27 for 511 pulses but divides 28 for the 512ns pulse

Figure 6.3.2.1: Time Chain Section

6.3.2.2 Spacecraft Time (SCTime) Section

6.3.2.2.1 Overview

The SCTime section contains the counters and registers used to set and read the spacecraft clock, as well as record the frame start

time, and generate the ARTI, RTI and the DEADP signals. Here, the frame start time means the time of the first frame of every DL buffer.

The spacecraft clock is functionally a 46 bit counter, which will keep track of time from 0 to 4,294,967,295.999 seconds (~136 years) in 61.031 microsecond intervals. The time format is split up into three sixteen bit words. Two of the three words represent the number of elapsed seconds, while the third word holds the elapsed subsecond count. Only the the most significant 14 bits of the last word are used and two least significant bits are ground permanently. These spacecraft time words are mapped to the registers 7, 8, and 9 of the RSDL.

When either elapsed second word is read, the actual value of the spacecraft time counters are driven directly onto the data bus. To prevent the subsecond counter transitions during a read of the subsecond data word, it's value is loaded in a buffer register. The subsecond buffer register is loaded continuously except during a subsecond word read, when the loading of the buffer is disabled. Thus, the user will get the spacecraft subsecond time exactly at the beginning of the memory read cycle of the subsecond register.

The subsecond word is also loaded into a separate frame start register when signalled by the RSDL. This register allows the RSDL hardware to record the start time of the first frame of every DL buffer. This value does not change until the DL buffer swaps. The frame start register can be read by the software.

The SCTime block also contains the RTI, ARTI, and DEADP signals. These signals are derived directly from the spacecraft clock. The RTI signal is derived from the 0 to 1 transition of the 1/8th second bit in the spacecraft clock. The ARTI signal is derived from the spacecraft time counter also and occurs approximately five milliseconds before the RTI signal. Both the ARTI and RTI signals have a ~1.004 microsecond pulse width. The DEADP signal is active from the end of the ARTI pulse to the beginning of the RTI pulse.

6.3.2.2.2 Spacecraft Time Sub-second Idiosyncrasies

In general, the simplest way of getting a high resolution real time clock would be to pick a sufficiently high power-of-two (2^N)

frequency to drive the LSB of a counter. Due to system frequency constraints the RSDL oscillator frequency is 11,944,800 Hz, this limits the highest power-of-two frequency obtainable to 32 Hz (1/32 second). Using this frequency to drive the LSB of a spacecraft time counter gives a clock that can resolve time down to 1/32 of a second. One of the two CDS clock counters is derived from this 32 Hz signal.

To be able to resolve times under 1/32nd of a second, another counter has to be driven by a higher power-of-two frequency then 32 Hz. Since none can be directly derived from the 11944800 Hz oscillator, a frequency was generated which is a pseudo 16384 Hz signal. This signal toggles exactly 512 times over a 1/32nd of a second time period (16348 times a second). Using this signal to drive a separate counter gives another 9 binary bits of spacecraft time resolution. To achieve this pseudo 16384 Hz signal, the period of one of the 512 time pulses is longer than the rest by a factor of 28/27 (see Figure 6.3.2.2.1).

Since this pseudo 16384 Hz signal is being used to force the transitions of the LSB of a counter, and since one of these 512 pulses has a longer period than the other pulses, one of the counter transitions will represent a longer time interval than other transitions. With the current design when this 9 bit counter transitions from 000000001_b to 000000010_b the time elapsed is ~63.291 microseconds. Every other transition occurs at an interval of ~61.030 microseconds. This allows for the subsecond count to be accurate (512 transitions equals exactly 1/32nd of a second) and deterministic for time measurements under 1/32 of a second. Figures 6.3.2.2.2 shows how these two counters are used to produce the 46 bit spacecraft time.

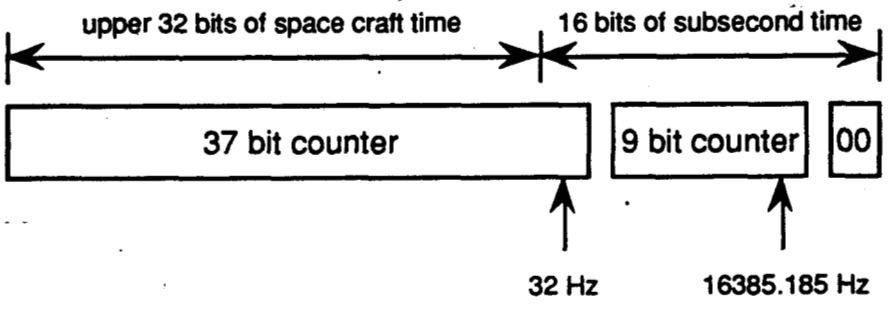


Figure 6.3.2.2.2: Partitioning of Spacecraft Time Counters

6.3.2.2.3 Spacecraft Time Loading and Cross String Synchronization

While the spacecraft clock time is loadable, only 32 of the 46 bits can be loaded. That is, the spacecraft time is only loadable to a 1 second resolution. The two word spacecraft time is loaded into holding registers, and is transferred to the actual spacecraft clock when time load conditions are met. Conditions for TU time loading are given the following truth table [12].

PRIME	Redundant String Health	Ground Update Enabled	S/W Update Enabled	S/C Time is loaded at next
true	don't care	true	true	RTI
false	true	*don't care*	true	XRTI
false	false	true	true	RTI

As shown in the above truth table, there are two timing signals which can be used to initiate spacecraft time loading, these are the RTI and XRTI signals. The RTI signal is generated in the TU and allows the time to be loaded on a second boundary (assuming software only allows a load on RTI#0). The XRTI signal is broadcast to the secondary CDS string from the prime CDS string and allows the secondary TU to synchronize it's time to the primary TU.

The Prime and Ground Update Enable inputs are CRC bits. The prime CRC bit decides if this string is the primary or secondary CDS string. The ground update enable CRC is used to indicate if the ground wishes to update spacecraft time. If the ground update bit is being used to allow a new time to be loaded, it must be set before and cleared after each new time is loaded. Multiple ground directed loads will not occur by leaving the ground update enable CRC set.

The redundant string health is a signal from the HCD, and reports on the redundant CDS string health. The S/W update enable bit is a bit in the TU control register of the RSDL ASIC. It is set by software to allow a new time to be loaded assuming all other conditions are met. It is automatically cleared when the spacecraft time is actually loaded.

When the TU is prime, and the Ground Update Enable CRC and software time update bit are set, the new two word time is loaded into the upper 32 bits of the spacecraft clock counter at the next RTI.

If the TU is secondary, the redundant string health is good, and the software time update bit is set, then at the next occurrence of the XRTI the new two word time is loaded into the upper 32 bits of the spacecraft clock counter and all subsecond bits are cleared. This allows for synchronization of the secondary with the prime string. This will occur regardless of the state of the ground update enable CRC.

If the TU is secondary, the redundant string health is bad, and the ground update enable and the software time update bits are set, then the new two word time is loaded into the upper 32 bits of the spacecraft clock counter at the next RTI. This allows for the ground to load the secondary from the ground when the prime string is bad.

6.3.2.3 Downlink Data Rate Generator Section

The DLGen block generates the DLOUT signal, which supplies the the RSDL with a X12 (times twelve) downlink data rate signal. This X12 signal is used in the generation of the downlink data transmission rate, which is 1/12th the frequency of the DLOUT signal. The DLGen has both a fixed and a programmable downlink data rate (see figure 6.3.2.3). The fixed data rate is automatically selected after a POR, and sets a downlink data transmission rate of 5 bits per a second (bps). In most cases the programmable data rate option will be used, this allows for downlink data transmission rates from 5 to 248,850 bps (corresponding to DLOUT frequencies of 60 to 2,986,200 bps) to be selected. The selection of a fixed or programmable data rate is controlled by a bit in the DLGen control register, which will be defined in more detail (as will all TU registers) in Section 6.2.

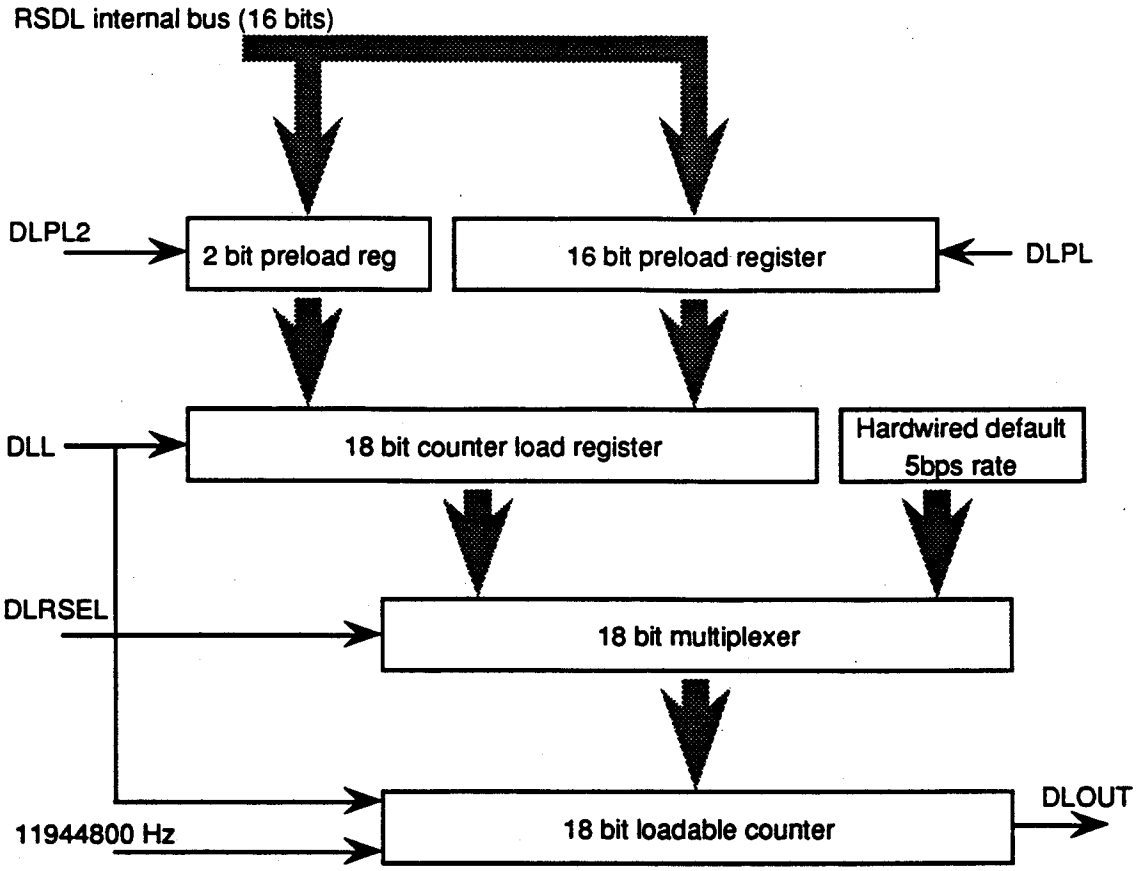


Figure 6.3.2.3: Downlink Data Rate Generator

The downlink generator was implemented as a software loadable frequency divider. This design takes the 11944800 Hz system frequency and divides it to the X12 frequency used by the RSDL. The frequency divider is a 18 bit wide counter which is loaded from the downlink preload registers. The downlink preload registers are two writeable word wide registers. By setting the downlink rate load bit in the TU control register, the divider value will be transfered form the preload registers to the downlink rate counter at the next RTI. There are predefined data rate frequencies to be used by the CDS, these data rates are a small subset of the data rates that this divider will generate. This divider will generate non-integer data rates if loaded with the improper values. All hardware-supported rates and its corresponding divisor values are given in Appendix B.

6.3.3. BA Block

The Bus Arbiter (BA) block provides all the logic for the ISB bus arbiter. It also generates control signals to enable 2A2 Board Address bus. Figure 6.3.3.a shows the timing diagram of theses control signals.

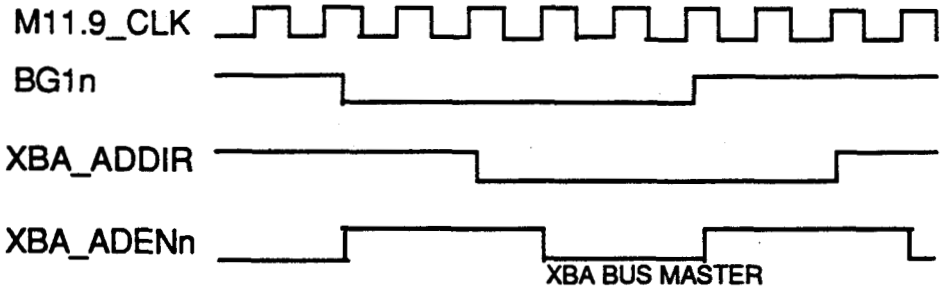


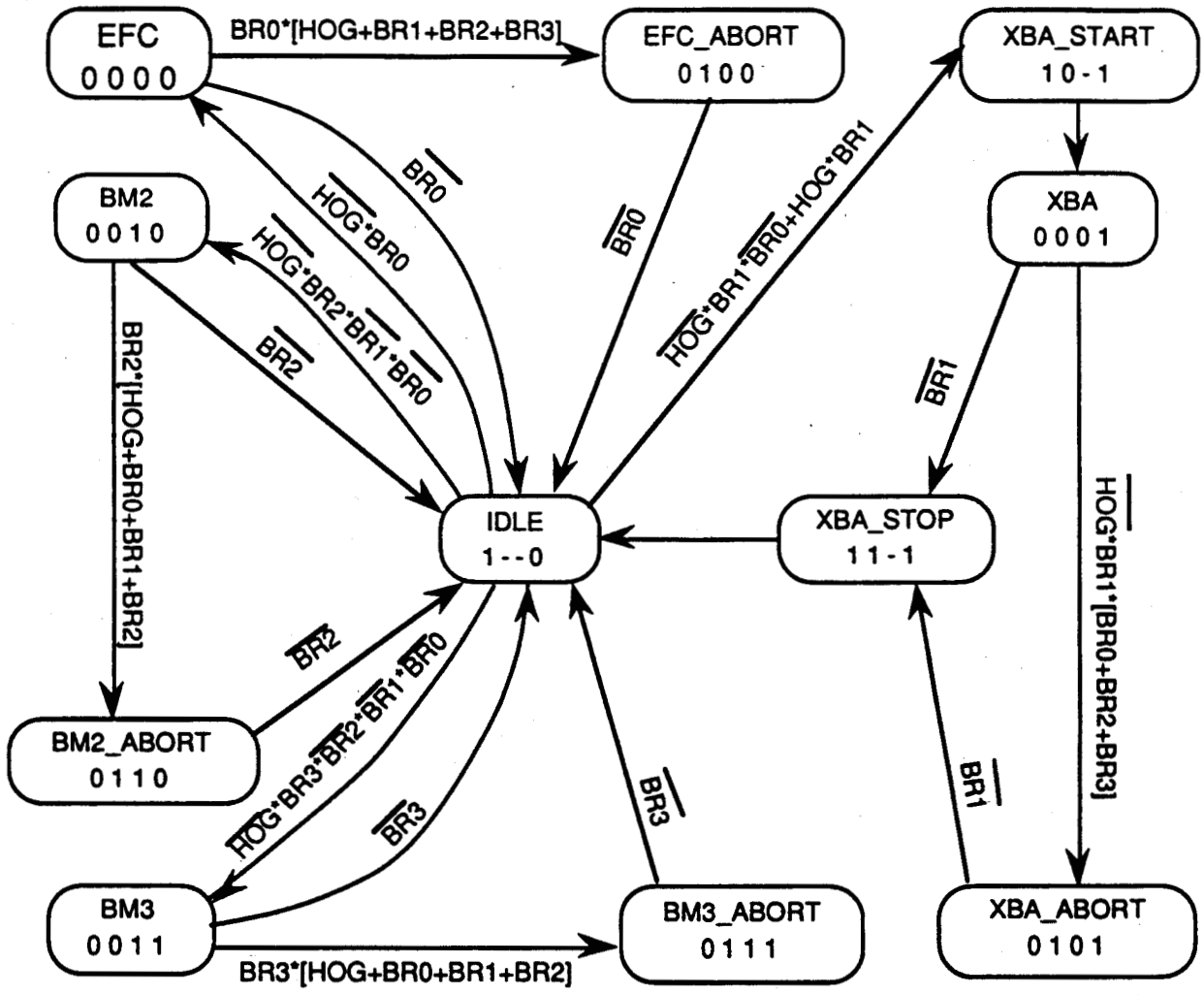
Figure 6.3.3.a Control signals of 2A2 Board Address Bus

The BA will perform bus arbitration for the ISB bus between four possible bus masters. Currently there are only two defined bus masters, the EFC and the cross strap bus adapter (XBA), but four such masters are incorporated in the ISB arbiter design as defined in the EFC specification (section 3.4.2.2.1).

Access to the ISB bus is requested via four bus request lines (BR0 - BR3), BR0 has has the highest priority while BR3 has the lowest priority. Access to the bus is granted by the corresponding bus grant lines (BG0 - BG3). The bus request and bus grant lines are active low.

The following sequence of events defines how a bus master achieves and maintains access to the EFC bus. A bus master asserts it's bus request signal. Sometime later the bus arbiter will assert the corresponding bus grant line. The bus master then has control of the bus until it deasserts it's request signal or it is signaled to get off the bus by the bus grant abort signal.

There are two distinct modes of the ISB arbiter. The first mode, which describes the arbitration of the ISB between the four bus masters under normal operating conditions, is referred to as normal mode. The second mode, which describes the "arbitration" of only the XBA bus master, is referred to as hog mode. This mode is only active when the hog line is asserted. These two modes of the arbiter state diagram are shown in Figure 6.3.3.b.



Note: XBA_ADDIR = 0 in "XBA states", otherwise 1
XBA_ADENn = 0 when any bus grant asserted
BGABTn = 0 when 1st MSB & 2nd MSB of state = 01, or when 1st MSB of state = 1

Figure 6.3.3.b Bus Arbiter State Diagram

Figure 6.3.3.b shows the allowable transitions between arbiter states. The state that the arbiter is in determines which bus master has the bus. The state that the arbiter is in controls the bus grant lines, while the transitions between states is controlled by the bus request lines.

While in normal access mode, the EFC has highest priority for bus access, the XBA has second priority and the two undefined bus masters have third and forth priorities.

While in normal access mode, all bus masters except the EFC are allowed to hold the bus as long as they can until a bus request from another bus master is received by the arbiter. Upon receiving the request, the arbiter will issue a bus abort. After the current bus master request line is deasserted, the bus arbiter will grant bus access to the higher priority bus master.

While in hog mode, the ISB arbiter will only grant the bus to the XBA bus master, all other bus master requests will not be recognized. The hog mode will be used only for support equipment access to the bus before launch.

6.3.4. Sync Pattern Block

A hardwired synchronization pattern is found in this block. The sync pattern is defined by CCSDS in [7] to be 1ACFFC1D. It will be shifted out serially (with the MSB first) to the RS Encoder block at the beginning of every DL frame.

6.3.5. RS Encoder Block

The encoder design is a modified version of the Mars Observer RS Encoder design. Several design modifications have been made to satisfy the C/C requirements.

Besides the RS encoder, this block includes a multiplexer to select input from either the Sync Pattern block or the SSRIU device. It interfaces directly with the RS memory buffer with internal addresses. Finally, it has capability to skip the RS encoding when the software specifies.

6.3.6. Timing & Control Block

This block generates timing and control used throughout the chip. It keeps track of the operational mode and the status of the RSDL chip. It provides logic to swap ping-pong buffers. It also provides logic to force the transfer frames to synchronize with a specified RTI and use a specified DL buffer when the synchronization occurs.

This block also captures the frame start time as follows. The Frame Start Register (Register 10) captures the exact time whenever the first bit of the first frame of the DL buffer is sent out. The relationship between the POR/Software Reset and the FST_CAP (first frame stamp capture) signal is shown in Figure 6.3.6a and the relationship between RTIn and FST_CAP is shown in Figure 6.3.6b.

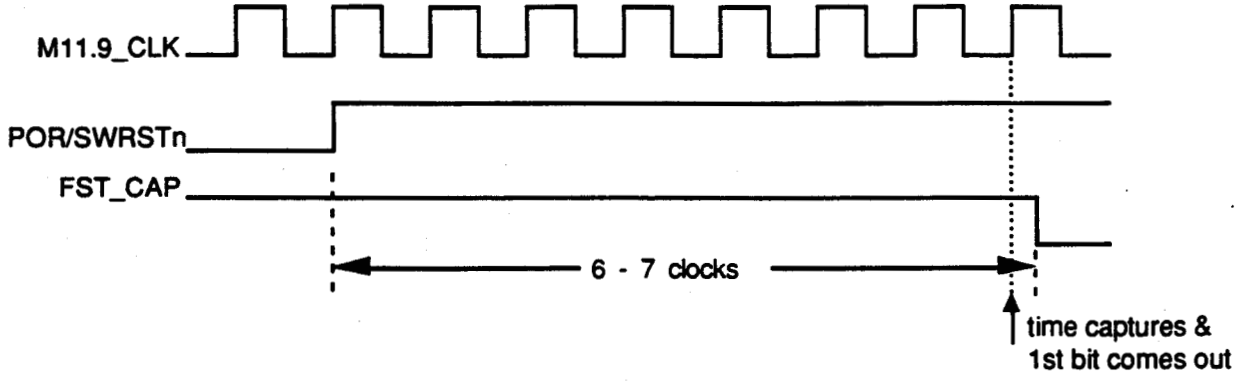


Figure 6.3.6a: Relationship between POR/SWRSTn & FST_CAP

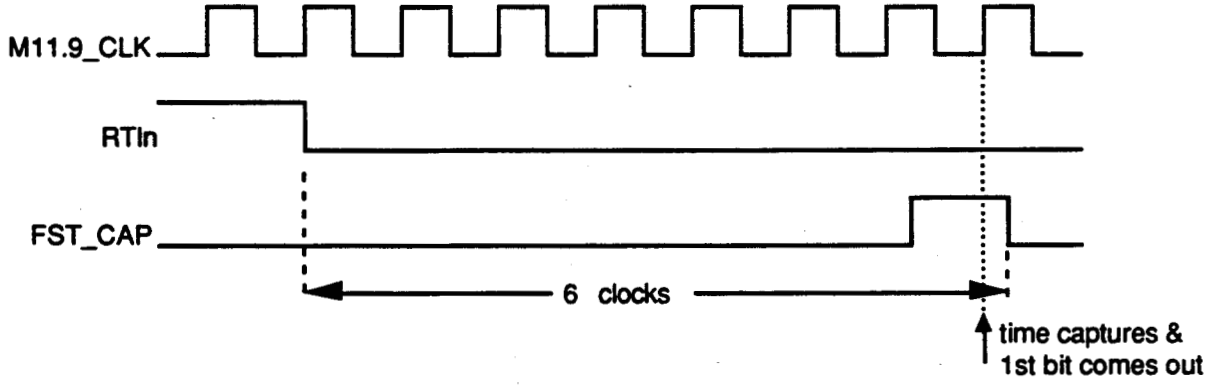


Figure 6.3.6b: Relationship between RTIn & FST_CAP

The first bit of the first frame is valid 6 to 7 clock cycles (≈500 to 586 ns) after reset and it is valid 6 clock cycles (≈500 ns) after RTIn.

6.4. Software Capabilities/Restrictions

The following are things that the software can do:

- Force hardware to synchronize the Transfer Frames with the next RTI (Sync RTI). In the event of TF out of sync, the last bit before the RTI could be shorter than normal.

- Inhibit or prohibit the RS encoding at the Sync RTI.
- Force hardware to use a specific buffer as the DL buffer at the Sync RTI.
- Enable/disable the DL buffer ping-pong.
- Specify the number of frames in the ping-pong buffers as well as the frame length.
- Specify the RS memory segment number used in the RS encoding. This segment number is only changed when the swap buffer occurs.
- Enable or disable individual interrupts.
- Change DL Data Rate. The new data rate will be used when RTI occurs. It is highly recommended to resynchronize TF at the same time when the new data rate takes in effect.
- Change S/C time. Only 32 MSB bits of the S/C time can be changed. The new S/C will be used when RTI/XRTI occurs.
- Get status of the RSDL device.

7. Software Considerations

Software has the responsibility to ensure that the time for collecting transfer frames is shorter than the time for sending transfer frames. However, the RSDL chip provides a capability for the software to disable the swapping of the DL buffer before the frame collection is not completed. The software can enable or disable the DL buffer swapping by setting Bit 1 of the register #0. If this bit is set when a buffer swap occurs, the hardware will swap to the new buffer and the bit is cleared subsequently. Otherwise, the Disabled Buffer Swap Interrupt will be issued, Bit 7 of the register #1 will be set, and the hardware will swap to the same buffer (swap on itself). The software can also mask the Disable Buffer Swap Interrupt by setting Bit 7 of the register #0 to one. A Begin Buffer Interrupt will always be issued whenever the buffer pointer points to the beginning of the buffer, regardless whether the swap has actually occured.

The Status, Control, and Interrupt registers use a special write scheme which allows the access of individual bits. Writing to these registers requires special attention.

The frames just before and after the synchronization of the output frames with the RTI could be corrupted. The previous frame may not be completed when the RTI comes. Also, it is possible that

the check bits might not be all cleared before the next transfer frame starts to be encoded. This will cause the check bits to be incorrect for the first frame after synchronization.

After PORn and software reset, all internal registers are at the states shown in the following tables:

States After PORn

Register	Value	Description
0	0x01F0	DL Buffer is set to A Buffer, all enable bits are reset, all interrupt masks are on, RSDL is in encoding mode. *(Note: For RSDL, mask bits are turned on when they are set to 1. This is different from other ASICs.)*
1	0x0110	The Disabled Buffer Swap Interrupt (Bit 7) and Begin Buffer Interrupt (Bit 11) are set and all other interrupts are cleared. Note: this value will changed to 0x0130 due to end-of-buffer approximately 6 seconds after POR.
2	0x0226	# of frames is 8, frame size is 550words.
3	0x0226	# of frames is 8, frame size is 550words.
4	0x0000	Segment 0 is used for RS encoding.
5,6	0x0000	32 MSB bits of the Load S/C time are cleared after PORn only.
7,8,9	Non-Resetable	48-bit S/C time. These registers are loaded by software and will not be reset by the PORn.
10	Non-Resetable	16 LSB bits of the S/C time when the Frame Start occurs. This register is loaded by software and will not be reset by the PORn.
11,12	0x0000	18-bit Downlink Data Rate is cleared and the DL rate is set to a predefined value 5bit/s after PORn only.

States After Software Reset

Register	Value	Description
0	0x01F0	DL Buffer is set to A Buffer, all enable bits are reset, all interrupt masks are on, RSDL is in encoding mode.

1	0x0110	The Disabled Buffer Swap Interrupt (Bit 7) and Begin Buffer Interrupt (Bit 11) are set and all other interrupts are cleared. Note: this value will change to 0x0130 in less than 6 seconds after software reset based on current DL rate.
2	0x0226	# of frames is 8, frame size is 550words.
3	0x0226	# of frames is 8, frame size is 550words.
4	0x0000	Segment 0 is used for RS encoding.
5,6	unchanged	The contents of these registers are not changed after software reset.
7,8,9	Non-Resetable	48-bit S/C time. These registers are loaded by software and will not be reset.
10	Non-Resetable	16 LSB bits of the S/C time when the Frame Start occurs. This register is loaded by software and will not be reset.
11,12	unchanged	The contents of these registers are not changed after software reset.

After reset, software needs to resynchronize Transfer Frames with next RTI, mask out unwanted interrupts, redefine if necessary # of frames in the DL Buffer, frame size, segment number, downlink data rate.

The RSDL chip generates downlink data rates ranged from 5bps to 248850bps. A table of all hardware-supported rates is shown in Appendix B. The TU block provides a 18-bit up counter to generate a 12 times downlink data rate which is used in the RS encoder. So, to get a downlink data rate of 11060bps,

12 times data rate: 132720

Divisor: 11944800/132720 = 90 or 0x5a

18-bit 2's complement: 0x3ffff - 0x5a = 0x3ffa6

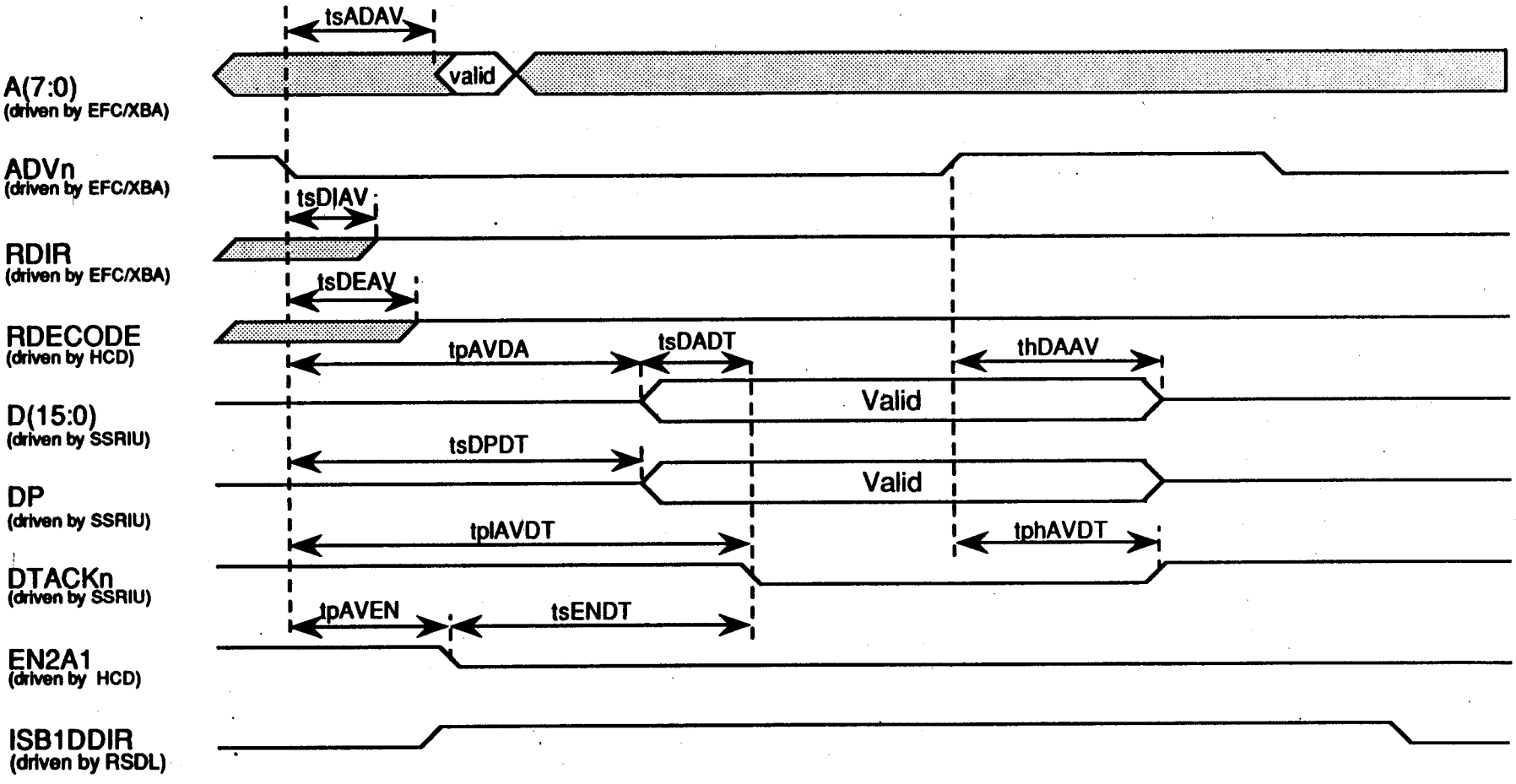
the value to be loaded to register #11 is 3 and

to register #12 is 0xffa6.

Appendix A

ISB Timing Diagrams

Figure A.1: ISB Read from RSDL Register, No Error

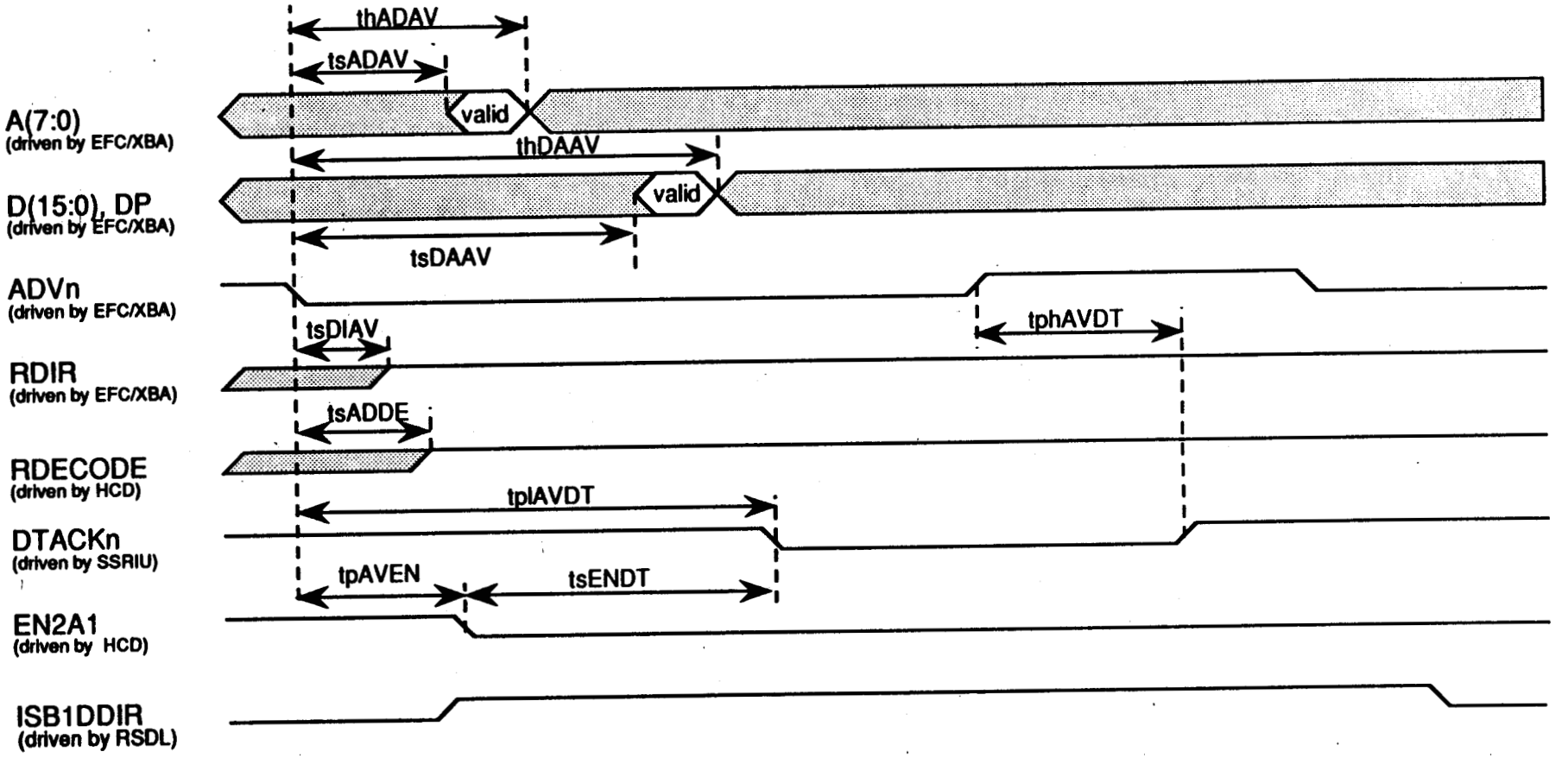


		Min	Max
tsADAV	Address setup after ADVn*	---	89 ns
thADAV	Address hold after ADVn	195 ns	---
tsDIAV	RDIRn stable after ADVn*	---	89 ns
tsDEAV	RDECODE stable after ADVn*	---	145 ns
tpAVDA	ADVn active to data valid	340 ns	434 ns
thDAAV	Data remains valid after ADVn deactivated	171 ns	265 ns
tpIAVDT	ADVn active to DTACKn active	425 ns	528 ns

		Min	Max
tsDADT	Data valid before DTACKn active	85 ns	94 ns
tphAVDT	ADVn deactivated to DTACKn deactivated	167 ns	260 ns
tsDPDT	Data parity (DP) stable before DTACKn	136 ns	144 ns
tpAVEN	ADVn to EN2A1 delay	84 ns	167 ns
tsENDT	EN2A1 setup before DTACKn	167 ns	333 ns

*Note: There are no requirements of how long these signals should be setup before ADVn

Figure A.2: ISB Write to RSDL Register, No Error

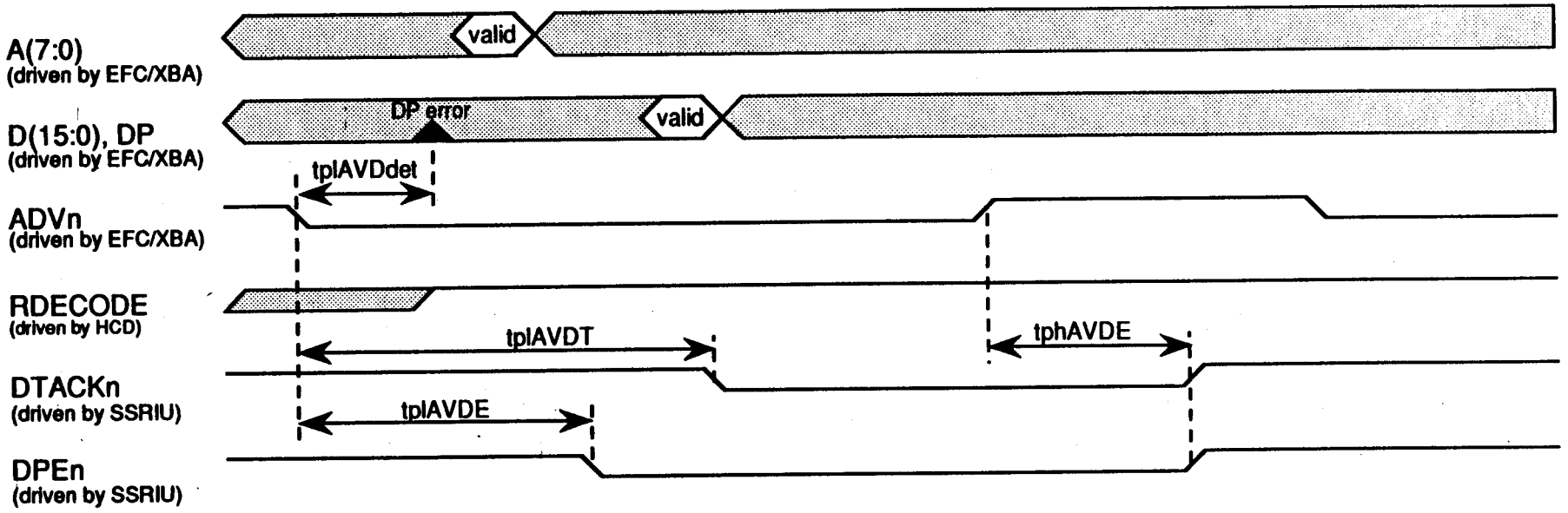


		Min	Max
tsADAV	Address setup after ADVn active*	---	89 ns
thADAV	Address hold after ADVn active	195 ns	---
tsDIAV	RDIRn stable after ADVn active*	---	89 ns
tsDEAV	RDECODE stable after ADVn active*	---	145 ns
tsDAAV	Data stable after ADVn active*	---	322 ns
thDAAV	Data hold after ADVn active	528 ns	---

		Min	Max
tplAVDT	ADVn active to DTACKn active	425 ns	528 ns
tphAVDT	ADVn deactivated to DTACKn deactivated	167 ns	260 ns
tpAVEN	ADVn to EN2A1 delay	0 ns	0 ns
tsENDT	EN2A1 setup before DTACK	333 ns	417 ns

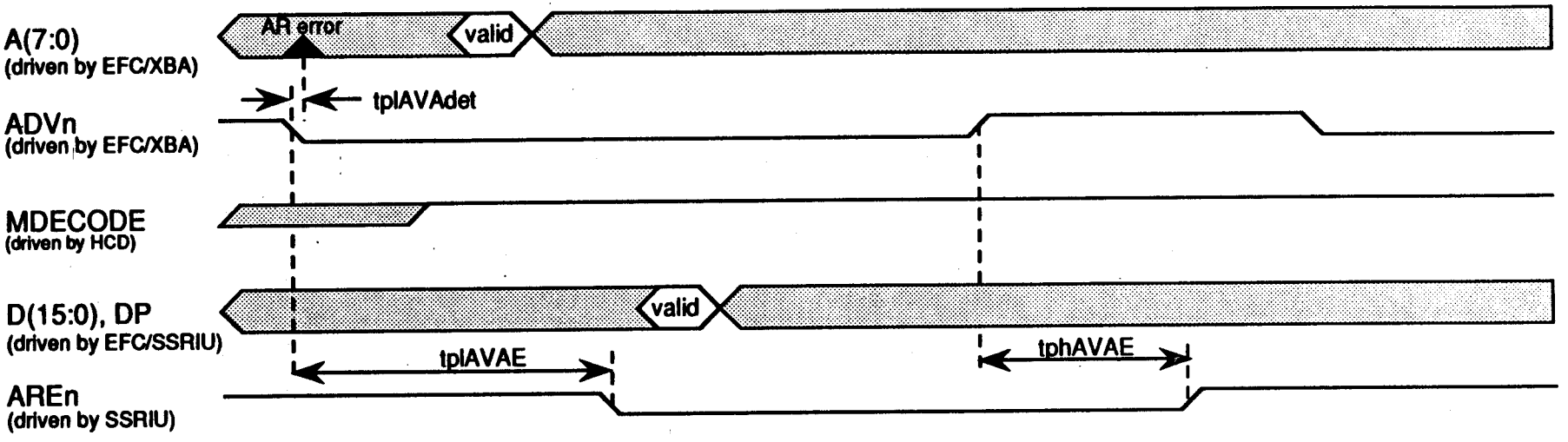
*Note: There is no requirements of how long these signal should be setup before ADVn

Figure A.3: ISB Write to RSDL Register, Data Parity Error



Parameter	Description	Min	Max
tplAVDE	ADVn active to data parity error (DPEn)	252 ns	336 ns
tplAVDdet	Parity error detected after ADVn active	37 ns	145 ns
tphAVDE	ADVn deactivated to DPEn deactivated	168 ns	253 ns
tplAVDT	ADVn active to DTACKn active	341 ns	444 ns

Figure A.4: ISB Read/Write to RSDL Register, Address Range Error



Parameter	Description	Min	Max
tplAVAdet	Addr range error detected after ADVn active	8 ns	11 ns
tplAVAE	ADVn to address range error (AREn) delay	252 ns	336 ns
tphAVAE	ADVn deactivated to AREn deactivated	168 ns	252 ns

Appendix B

Downlink Data Rates Supported by RSDL ASIC

C/C DOWNLINK DATA RATE
INPUT FREQUENCY = 11944800.0
RTI FREQUENCY = 8.0
FRAME LENGTH = 10112

DIV BY	2'S COMPLEMENT(HEX)	DATA RATE	REPETITION
4	3fffc	248850.0	512
5	3fffb	199080.0	128
6	3fffa	165900.0	256
7	3fff9	142200.0	128
8	3fff8	124425.0	1024
9	3fff7	110600.0	128
10	3fff6	99540.0	256
12	3fff4	82950.0	512
14	3fff2	71100.0	256
15	3fff1	66360.0	128
18	3ffee	55300.0	256
20	3ffec	49770.0	512
21	3ffeb	47400.0	128
24	3ffe8	41475.0	1024
25	3ffe7	39816.0	128
28	3ffe4	35550.0	512
30	3ffe2	33180.0	256
35	3ffdd	28440.0	128
36	3ffdc	27650.0	512
40	3ffd8	24885.0	1024
42	3ffd6	23700.0	256
45	3ffd3	22120.0	128
50	3ffce	19908.0	256
56	3ffc8	17775.0	1024
60	3ffc4	16590.0	512
63	3ffc1	15800.0	128
70	3ffba	14220.0	256
72	3ffb8	13825.0	1024
75	3ffb5	13272.0	128
79	3ffb1	12600.0	10112
84	3ffac	11850.0	512
90	3ffa6	11060.0	256
100	3ff9c	9954.0	512
105	3ff97	9480.0	128
120	3ff88	8295.0	1024
126	3ff82	7900.0	256
140	3ff74	7110.0	512
150	3ff6a	6636.0	256
158	3ff62	6300.0	20224
168	3ff58	5925.0	1024
175	3ff51	5688.0	128
180	3ff4c	5530.0	512
200	3ff38	4977.0	1024
210	3ff2e	4740.0	256
225	3ff1f	4424.0	128
237	3ff13	4200.0	10112
252	3ff04	3950.0	512
280	3fee8	3555.0	1024
300	3fed4	3318.0	512
315	3fec5	3160.0	128
316	3fec4	3150.0	40448
350	3fea2	2844.0	256
360	3fe98	2765.0	1024

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395	3fe75	2520.0	10112
420	3fe5c	2370.0	512
450	3fe3e	2212.0	256
474	3fe26	2100.0	20224
504	3fe08	1975.0	1024
525	3fdf3	1896.0	128
553	3fdd7	1800.0	10112
600	3fda8	1659.0	1024
630	3fd8a	1580.0	256
632	3fd88	1575.0	80896
700	3fd44	1422.0	512
711	3fd39	1400.0	10112
790	3fcea	1260.0	20224
840	3fcb8	1185.0	1024
900	3fc7c	1106.0	512
948	3fc4c	1050.0	40448
1050	3fbe6	948.0	256
1106	3fbae	900.0	20224
1185	3fb5f	840.0	10112
1260	3fb14	790.0	512
1400	3fa88	711.0	1024
1422	3fa72	700.0	20224
1575	3f9d9	632.0	128
1580	3f9d4	630.0	40448
1659	3f985	600.0	10112
1800	3f8f8	553.0	1024
1896	3f898	525.0	80896
1975	3f849	504.0	10112
2100	3f7cc	474.0	512
2212	3f75c	450.0	40448
2370	3f6be	420.0	20224
2520	3f628	395.0	1024
2765	3f533	360.0	10112
2844	3f4e4	350.0	40448
3150	3f3b2	316.0	256
3160	3f3a8	315.0	80896
3318	3f30a	300.0	20224
3555	3f21d	280.0	10112
3950	3f092	252.0	20224
4200	3ef98	237.0	1024
4424	3eeb8	225.0	80896
4740	3ed7c	210.0	40448
4977	3ec8f	200.0	10112
5530	3ea66	180.0	20224
5688	3e9c8	175.0	80896
5925	3e8db	168.0	10112
6300	3e764	158.0	512
6636	3e614	150.0	40448
7110	3e43a	140.0	20224
7900	3e124	126.0	40448
8295	3df99	120.0	10112
9480	3daf8	105.0	80896
9954	3d91e	100.0	20224
11060	3d4cc	90.0	40448
11850	3d1b6	84.0	20224
12600	3cec8	79.0	1024
13272	3cc28	75.0	80896
13825	3c9ff	72.0	10112
14220	3c874	70.0	40448
15800	3c248	63.0	80896

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16590	3bf32	60.0	20224
17775	3ba91	56.0	10112
19908	3b23c	50.0	40448
22120	3a998	45.0	80896
23700	3a36c	42.0	40448
24885	39ecb	40.0	10112
27650	393fe	36.0	20224
28440	390e8	35.0	80896
33180	37e64	30.0	40448
35550	37522	28.0	20224
39816	36478	25.0	80896
41475	35dfd	24.0	10112
47400	346d8	21.0	80896
49770	33d96	20.0	20224
55300	327fc	18.0	40448
66360	2fcc8	15.0	80896
71100	2ea44	14.0	40448
82950	2bbfa	12.0	20224
99540	27b2c	10.0	40448
110600	24ff8	9.0	80896
124425	219f7	8.0	10112
142200	1d488	7.0	80896
165900	177f4	6.0	40448
199080	f658	5.0	80896

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